Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A non-volatile memory comprising:

an array of non-volatile memory cells; and

a stack controller coupled to receive an address and to determine an appropriate address for accessing values in a stack stored in a subset of the array of non-volatile memory cells, the stack having a stack depth configured in a nonvolatile memory to store parameter values, where each memory write invalidates previous data and further wherein the stack controller increments ~~updates~~ a pointer to a first valid word in the stack, the stack controller to maintain the stack utilizing two blocks of the non-volatile memory cells and to cause a first block to be erased when each word within the first block is invalid and the values in the stack are stored in a second block of the non-volatile memory.

2. (Previously Presented) The non-volatile memory of claim 1 wherein the first block and the second block are erased independently.

3-4. (Canceled)

5. (Currently Amended) The non-volatile memory of claim 1~~, the stack~~

~~controller further~~ including a register to store an offset value used to generate an address for words in the nonvolatile memory.

6. (Canceled)

7. (Previously Presented) The non-volatile memory of claim 1, wherein the stack controller is configured to distribute write cycles across multiple blocks of the nonvolatile memory.

8-10. (Canceled)

11. (Currently Amended) A method to manage a stack in a non-volatile memory having an array of cells logically organized as blocks, the method comprising:

receiving an address corresponding to an access to the stack;

maintaining a nonvolatile stack to store parameter values in words of a nonvolatile memory where a write of the nonvolatile stack invalidates previous instructions or data stored in the nonvolatile stack;

incrementing ~~updating~~ a pointer to a first valid word in the stack

maintaining the stack utilizing two blocks of the non-volatile memory cells and to cause a first block to be erased when each word within the first block is invalid and the values in the stack are stored in a second block of the non-volatile memory.

12. (Previously Presented) The method of claim 11 wherein a memory pool in

at least first and second blocks of the nonvolatile memory are sized to balance cycling and data retention capabilities with a write specification.

13. (Previously Presented) The method of claim 11 further comprising distributing write cycles across multiple blocks of the nonvolatile memory.

14. (Previously Presented) The method of claim 11 wherein the nonvolatile memory maps a received address to determine memory blocks to be written.

15-31. (Canceled)

32. (Previously Presented) The stack of claim 1 wherein the nonvolatile memory is a polymer memory that includes ferroelectric memory cells.